TISP4C115H3BJ THRU TISP4C395H3BJ

LOW CAPACITANCE BIDIRECTIONAL THYRISTOR OVERVOLTAGE PROTECTORS

TISP4CxxxH3BJ Overvoltage Protector Series

Ion-Implanted Breakdown Region
- Precise and Stable Voltage
- Low Voltage Overshoot under Surge
- Low Off-State Capacitance

Device Name	V_{DRM} V	$V_{(BO)}$ V
TISP4C115H3BJ †	90	115
TISP4C125H3BJ †	100	125
TISP4C145H3BJ †	120	145
TISP4C165H3BJ	135	165
TISP4C180H3BJ †	145	180
TISP4C220H3BJ †	180	220
TISP4C250H3BJ †	190	250
TISP4C290H3BJ †	220	290
TISP4C350H3BJ †	275	350
TISP4C395H3BJ †	320	395

Rated for International Surge Wave Shapes

Wave Shape	Standard	I_{PPSM} A
2/10	GR-1089-CORE	500
10/160	TIA-968-A	200
10/700	ITU-T K.20/21/45	150
10/560	TIA-968-A	100
10/1000	GR-1089-CORE	100

SMB Package (Top View)

Device Symbol

† ..... **UL Recognized Component**

Description

This device is designed to limit overvoltages on the telephone line. Overvoltages are normally caused by a.c. power system or lightning flash disturbances which are induced or conducted on to the telephone line. A single device provides 2-point protection and is typically used for the protection of 2-wire telecommunication equipment (e.g. between the Ring and Tip wires for telephones and modems). Combinations of devices can be used for multi-point protection (e.g. 3-point protection between Ring, Tip and Ground).

The protector consists of a symmetrical voltage-triggered bidirectional thyristor. Overvoltages are initially clipped by breakdown clamping until the voltage rises to the breakover level, which causes the device to crowbar into a low-voltage on state. This low-voltage on state causes the current resulting from the overvoltage to be safely diverted through the device. The high crowbar holding current prevents d.c. latchup as the diverted current subsides.

Please contact your Bourns representative if the protection voltage you require is not listed.

How to Order

Device	Package	Carrier	Order As	Marking Code	Std. Qty.
TISP4CxxxH3BJ	SMB	Embossed Tape Reeled	TISP4CxxxH3BJR-S	4CxxxH	3000

Insert xxx corresponding to device name.

*RoHS Directive 2002/95/EC Jan 27 2003 including Annex
SEPTEMBER 2004 – REVISED JUNE 2007
Specifications are subject to change without notice.
Customers should verify actual device performance in their specific applications.

Absolute Maximum Ratings, T_A = 25 °C (Unless Otherwise Noted)

Rating		Symbol	Value	Unit
Repetitive peak off-state voltage	'4C115H3BJ	V_{DRM}	±90	V
	'4C125H3BJ		±100	
	'4C145H3BJ		±120	
	'4C165H3BJ		±135	
	'4C180H3BJ		±145	
	'4C220H3BJ		±180	
	'4C250H3BJ		±190	
	'4C290H3BJ		±220	
	'4C350H3BJ		±275	
	'4C395H3BJ		±320	
Non-repetitive peak impulse current (see Notes 1 and 2)		I_{PPSM}		A
2/10 µs (GR-1089-CORE, 2/10 µs voltage wave shape)			±500	
10/160 µs (TIA-968-A, 10/160 µs voltage wave shape)			±200	
5/310 µs (ITU-T K.44, 10/700 µs voltage wave shape used in K.20/21/45)			±150	
10/560 µs (TIA-968-A, 10/560 µs voltage wave shape)			±100	
10/1000 µs (GR-1089-CORE, 10/1000 µs voltage wave shape)			±100	
Non-repetitive peak on-state current (see Notes 1, 2 and 3)		I_{TSM}		A
20 ms, 50 Hz (full sine wave)			30	
1000 s, 50 Hz			2.1	
Junction temperature		T_J	-40 to +150	°C
Storage temperature range		T_{stg}	-65 to +150	°C

NOTES: 1. Initially the device must be in thermal equilibrium with T_J = 25 °C.
2. The surge may be repeated after the device returns to its initial conditions.
3. EIA/JESD51-2 environment and EIA/JESD51-3 PCB with standard footprint dimensions connected with 5 A rated printed wiring track widths.

Electrical Characteristics, T_A = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions		Min	Typ	Max	Unit
I_{DRM}	Repetitive peak off-state current	$V_D = V_{DRM}$	T_A = 25 °C			±5	µA
			T_A = 85 °C			±10	
$V_{(BO)}$	Breakover voltage	dv/dt = ±250 V/ms, R_{SOURCE} = 300 Ω	'4C115H3BJ			±115	V
			'4C125H3BJ			±125	
			'4C145H3BJ			±145	
			'4C165H3BJ			±165	
			'4C180H3BJ			±180	
			'4C220H3BJ			±220	
			'4C250H3BJ			±250	
			'4C290H3BJ			±290	
			'4C350H3BJ			±350	
			'4C395H3BJ			±395	
$V_{(BO)}$	Impulse breakover voltage	dv/dt ≤ ±1000 V/µs, Linear voltage ramp, Maximum ramp value = ±500 V di/dt = ±10 A/µs, Linear current ramp, Maximum ramp value = ±10 A	'4C115H3BJ			±125	V
			'4C125H3BJ			±135	
			'4C145H3BJ			±155	
			'4C165H3BJ			±175	
			'4C180H3BJ			±190	
			'4C220H3BJ			±230	
			'4C250H3BJ			±260	
			'4C290H3BJ			±300	
			'4C350H3BJ			±360	
			'4C395H3BJ			±405	
$I_{(BO)}$	Breakover current	dv/dt = ±250 V/ms, R_{SOURCE} = 300 Ω				±600	mA
V_T	On-state voltage	I_T = ±5 A,t_w = 100 µs				±3	V
I_H	Holding current	I_T = ±5 A, di/dt = ±30 mA/ms		±150		±600	mA
C_O	Off-state capacitance	f = 1 MHz, V_d = 1 V rms, V_D = -2 V	'4C115H3BJ '4C125H3BJ			50	pF
			'4C145H3BJ '4C165H3BJ '4C180H3BJ '4C220H3BJ '4C250H3BJ			45	
			'4C290H3BJ '4C350H3BJ '4C395H3BJ			40	

Thermal Characteristics, T_A = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
$R_{\theta JA}$	Junction to ambient thermal resistance	EIA/JESD51-3 PCB, $I_T = I_{TSM(1000)}$ (see Note 4)			113	°C/W
		265 mm x 210 mm populated line card, 4-layer PCB, $I_T = I_{TSM(1000)}$		50		

NOTE: 4. EIA/JESD51-2 environment and PCB has standard footprint dimensions connected with 5 A rated printed wiring track widths.

Parameter Measurement Information

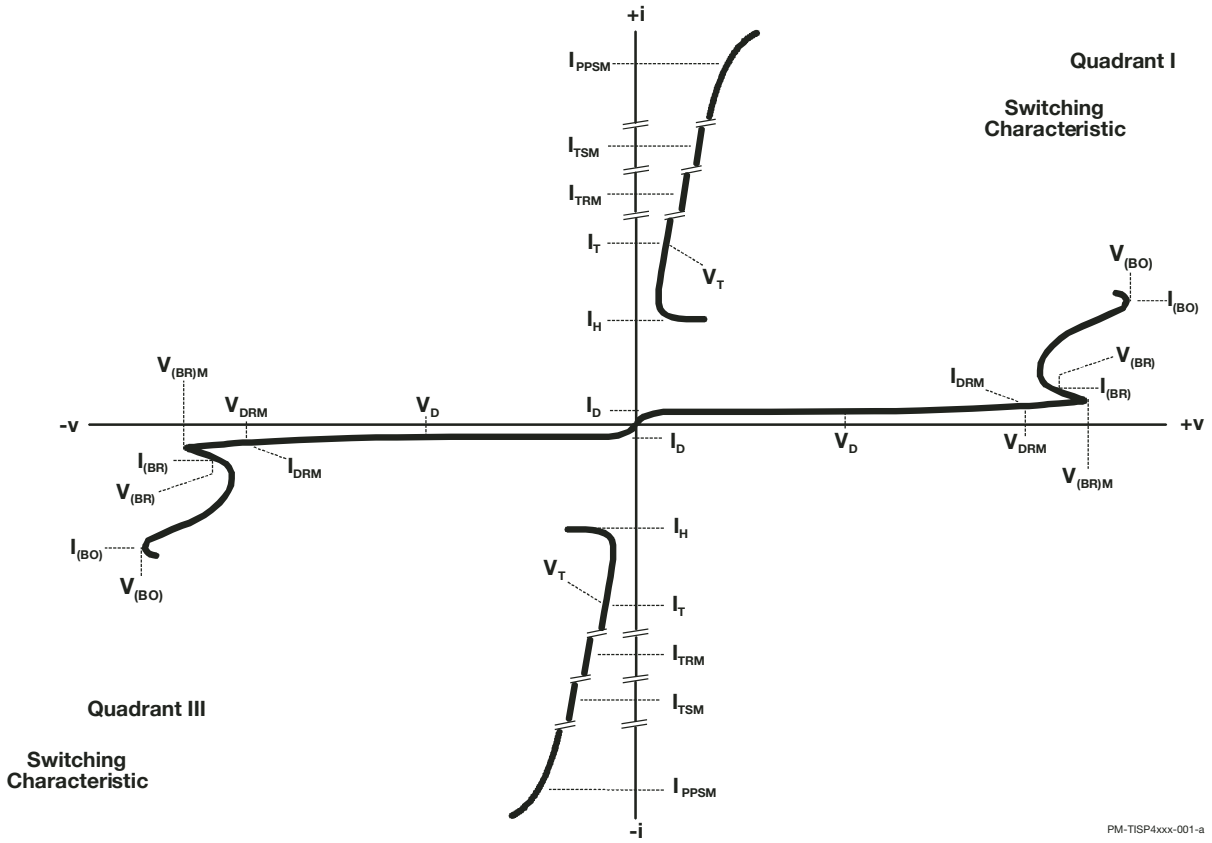

Figure 1. Voltage-Current Characteristic for T and R Terminals
All Measurements are Referenced to the R Terminal

Typical Characteristics